WHAT IS CLAIMED IS:

1. A process for self-aligned manufacturing integrated electronic devices, comprising the steps of:

- forming, in a semiconductor wafer having a substrate, insulation structures delimiting active areas and projecting from said substrate;

- forming a first conductive layer coating said insulation structures and said active areas; and

- partially removing said first conductive layer;

wherein, prior to forming said first conductive layer, forming recesses in said insulation structures.

2. The process according to claim 1 wherein said step of forming said first conductive layer comprises filling said insulation structures.

3. The process according to claim 1 wherein said step of forming recesses comprises removing side portions of said insulation structures so as to form first recesses.

4. The process according to claim 3 wherein said first recesses are defined on top and at the side of respective ones of said active areas.

5. The process according to claim 3 wherein said step of partially removing comprises forming first conductive regions, which extend inside at least one of said first recesses and on top of a respective said active area.

6. The process according to claim 5 wherein said first conductive regions are floating gates of respective first memory cells.

7. The process according to claim 1 wherein said step of forming recesses comprises removing central portions of said insulation structures so as to form second recesses.

8. The process according to claim 7 wherein said second recesses are delimited laterally and at the bottom by respective ones of said insulation structures.

9. The process according to claim 8 wherein said step of partial removing comprises forming second conductive regions accommodated inside respective ones of said second recesses.

10. The process according to claim 9 wherein said second conductive regions comprise resistors.

11. The process according to claim 9 wherein second conductive regions comprise first plates of respective capacitors.

12. The process according to claim 1 wherein said step of forming recesses comprises performing at least one first masked etch of said insulation structures.

13. The process according to claim 12 wherein said step of forming recesses comprises performing a second masked etch of said insulation structures.

14. The process according to claim 1 wherein said step of partially removing comprises planarizing said wafer.

15. The process according to claim 1 wherein said step of partially removing is followed by the steps of:

- forming a dielectric layer on top of said wafer;
- forming a second conductive layer on top of said dielectric layer; and
- selectively removing said dielectric layer and said second conductive layer.

16. The process according to claim 15 wherein said step of selectively removing comprises forming third conductive regions.

17. The process according to claim 6, wherein said third conductive regions comprise control gates of said memory cells.

18. The process according to claim 11 wherein said third conductive regions comprise second plates of said capacitors.

19. An integrated electronic device comprising:

- a semiconductor body having a substrate; and
- a plurality of insulation structures delimiting active areas and having respective portions projecting from said substrate; wherein said insulation structures have respective recesses, which accommodate at least partially conductive regions.

20. The device according to claim 19 wherein said recesses are defined laterally with respect to respective projecting portions of said insulation structures.

21. The device according to claim 19 wherein said conductive regions comprise terminals of memory cells arranged on top of respective said active areas and extending laterally inside at least one of said recesses.

22. The device according to claim 19 wherein said recesses are defined centrally with respect to respective said projecting portions of said insulation structures.

23. The device according to claim 22 wherein said conductive regions are entirely accommodated inside respective said recesses.

24. The device according to claim 22 wherein said conductive regions comprise resistors.

25. The device according to claim 22 wherein said conductive regions comprise first plates of capacitors.

26. An integrated circuit, comprising:

a substrate having an active region;

first and second insulators disposed adjacent to the active region and defining a recess over a portion of the active region and over a portion of one of the insulators; and

a first conductor disposed in the recess.

27. The integrated circuit of claim 26 wherein the first and second insulators respectively comprise first and second projections that define the recess.

28. The integrated circuit of claim 26, further comprising:

first and second trenches disposed in the substrate; and

wherein the first and second insulators are respectively disposed in the first and second trenches.

29. The integrated circuit of claim 26 wherein the first and second insulators define the recess over respective portions of both the first and second insulators.

30. The integrated circuit of claim 26, further comprising a third insulator disposed between the first conductor and the active region of the substrate.

31. The integrated circuit of claim 26 wherein the active region and the conductor compose a memory cell.

32. The integrated circuit of claim 26 wherein the conductor composes a floating gate of a nonvolatile memory cell.

33. The integrated circuit of claim 26, further comprising:

a third insulator disposed on the first conductor; and

a second conductor disposed on the third insulator and overlapping the first conductor.

34. An integrated circuit, comprising:
a substrate;
a first insulator disposed in the substrate and defining a recess; and
a first conductor disposed in the recess.

35. The integrated circuit of claim 34 wherein the first insulator comprises projections that define the recess.

36. The integrated circuit of claim 34, further comprising:
a trench disposed in the substrate; and
wherein the first insulator is disposed in the trench.

37. The integrated circuit of claim 34 wherein the first conductor composes a resistor.

38. The integrated circuit of claim 34 wherein the first conductor composes a plate of a capacitor.

39. The integrated circuit of claim 34, further comprising:
a second insulator disposed on the first conductor; and
a second conductor disposed on the second insulator and overlapping the first conductor.

40. A method, comprising:
forming first and second insulators in a substrate;
forming a recess in a portion of one of the insulators and over a region of the substrate located adjacent to the first and second insulators; and
forming a first conductor in the recess.

41. The method of claim 40 wherein forming the first and second insulators comprises:
forming first and second trenches in the substrate; and
forming an insulating material in the trenches.

42. The method of claim 40 wherein forming the recess comprises forming the recess in respective portions of the first and second insulators.

43. The method of claim 40, further comprising forming a third insulator on the region of the substrate located adjacent to the first and second insulators.

44. The method of claim 40, further comprising:
forming a third insulator on the first conductor; and

forming a second conductor on the third insulator and overlapping the first conductor.

45. A method, comprising:
forming a first insulator in a substrate;
forming a recess in the first insulator; and
forming a first conductor in the recess.

46. The method of claim 45 wherein forming the first insulator comprises:
forming a trench in the substrate; and
forming an insulator material in the trench.

47. The method of claim 45, further comprising forming a second insulator on the first conductor.

48. The method of claim 45, further comprising:
forming a second insulator on the first conductor; and
forming a second conductor on the second insulator.